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Title: PITCH SHIFT APPARATUS. ;

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ABSTRACT:

This invention is concerned with pitch shift apparatus for converting an audio signal into PCM digital data and then making a pitch shift, wherein the PCM digital data is written in a ring memory (2) by a write address generator circuit (3), and read therefrom by two read address generator circuits (4, 5) which start to read at time points differing by an amount corresponding to 1/2 the ring memory (2) at a certain pitch, in which case immediately before the read address on the now finally outputting side and the write address causes passing or cyclic delay, the read address on the switching-to side is stopped from increasing during the interval from a time point at which an audio signal on the switching-to side makes zero crossing to a time at which an audio signal on the now outputting side makes in-phase zero crossing, and switching is made at the zero crossing point, so that the connection of the audio signals can be smoothly made without such AM modulated component as caused in the cross fade method, enabling high-quality pitch shift to be achieved.

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(54) **Pitch shift apparatus.**

(57) This invention is concerned with pitch shift apparatus for converting an audio signal into PCM digital data and then making a pitch shift, wherein the PCM digital data is written in a ring memory (2) by a write address generator circuit (3), and read therefrom by two read address generator circuits (4, 5) which start to read at time points differing by an amount corresponding to 1/2 the ring memory (2) at a certain pitch, in which case immediately before the read address on the now finally outputting side and the write address causes passing or cyclic delay, the read address on the switching-to side is stopped from increasing during the interval from a time point at which an audio signal on the switching-to side makes zero crossing to a time at which an audio signal on the now outputting side makes in-phase zero crossing, and switching is made at the zero crossing point, so that the connection of the audio signals can be smoothly made without such AM modulated component as caused in the cross fade method, enabling high-quality pitch shift to be achieved.

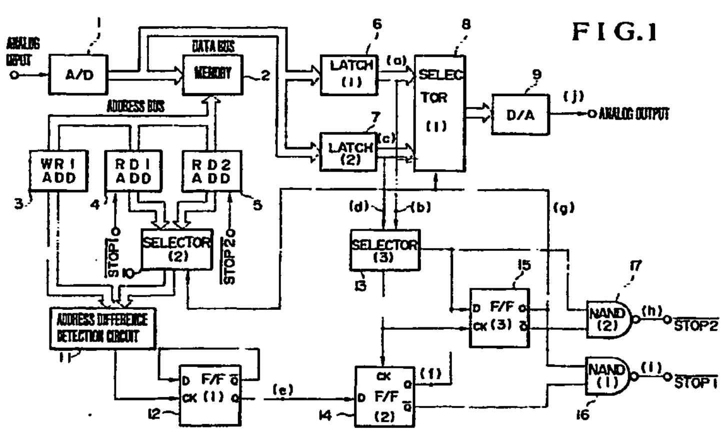

FIG.1

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BACKGROUND OF THE INVENTION

This invention relates to pitch shift apparatus and particularly to one in which analog audio signals are converted into PCM (pulse code modulation) digital data and then pitch shifted.

Recently, the audio signal processing technique has been greatly developed, and the digital signal processing technique is used to achieve high performance and high precision.

The pitch shift apparatus has been improved in its performance and precision by the use of the digital processing technique as the electronic musical instruments and vocal trainers (KARAOKE) have been widely used and developed. The conventional pitch shift apparatus has used the ADM (adaptive delta modulation) system as an A/D (analog/digital) approach for converting analog signals into digital signals in order to reduce the circuit scale and the cost, and made the pitch process and D/A (digital/analog) conversion on the ADM (Adaptive Delta Modulation) digital data to thereby produce analog audio signals (see the Institute of Electronics and Communication Engineers of Japan, EA95-40, issued 1985, 9.26).

In this conventional ADM system pitch shift apparatus, however, satisfactory performance could not be achieved. In recent years, the ADM system has almost been replaced by the PCM (pulse code modulation) as the A/D conversion approach, because the S/N, distortion, and lineality in the A/D conversion of the PCM system has been greatly improved with the development of the digital technology.

One example of the conventional PCM system pitch shift apparatus will hereinafter be described.

Fig. 3 is a block diagram of a conventional pitch shift apparatus, and Fig. 4 is an explanatory diagram for the explanation of the basic principle of the pitch shift operation, Fig. 5 is a schematic diagram useful for explaining the addresses of a memory in and from which writing and reading are made, and Fig. 6 is a waveform diagram showing the operation of each portion of the pitch shift apparatus of Fig. 3.

Referring to Fig. 3, there are shown an A/D converter 1, a memory 2, a memory write address generator circuit (WR1 ADD) 3, a first memory read address generator circuit (RD1 ADD) 4, a second memory read address generator circuit (RD2 ADD) 5, D/A converters 9, 18, attenuators 19, 20, and an adder 21. The operation of the pitch shift apparatus will be mentioned with reference to the drawings.

As illustrated in Fig. 3, an analog audio signal is supplied via an input terminal to the A/D converter 1, where it is sampled at a sampling frequency fs and converted into a PCM digital signal. This PCM digital signal is sequentially written in the memory 2 at the addresses specified by the memory write address generator circuit 3. The memory 2 is formed of a RAM (random access memory) as a ring memory. As shown in Fig. 5, the address begins at 0-address, increases at the frequency fs until the maximum, and again begins at 0-address.

The first memory read address generator circuit 4 is constructed to increase the address at intervals different from those of the memory write address generator circuit 3. The timing (intervals of time) for the reading is made as follows. For example, to increase the pitch, the intervals of time are made shorter than 1/fs [sec] (write timing (interval of time)), and to decrease the pitch, the intervals of time are made longer than 1/fs [sec]. Fig. 4 shows the change of the audio signal waveform for the decrease of the pitch. From Fig.4 it will be understood that the read timing T2 is longer than the write timing T1 (1/fs), or that the pitch-shifted waveform (Fig. 4b) has a frequency lower than that of the original waveform (Fig. 4a), or that the pitch is reduced.

The second memory read address generator circuit is constructed to generate the address which is spaced by an amount corresponding to 1/2 the ring memory from the address which the first read address generator circuit 4 generates. The PCM digital data read from the address specified by the first memory address generator circuit 4 is supplied to the D/A converter 9, and the PCM digital data read from the address specified by the second memory address generator circuit 5 is fed to the D/A converter 18. The outputs from the D/A converters 9, 18 are respectively supplied through the weighting attenuators 19, 20 to the adder 21, which produces the final pitch-shifted output (analog audio signal).

In this pitch shift apparatus, however, the amplitude of the pitch-converted output is not constant (see Fig. 6e), or an amplitude-modulated analog audio signal is obtained, so that a sine wave input with a constant amplitude results in offensive sound. In other words, since the timing T1 of the address from the memory write address generator circuit 3 is different from that T2 of the address from the first and second memory read address generator circuit 4, 5, the two addresses pass each other, or are delayed in cycles from each other with a constant period as time elapses. At this time, the PCM digital data read from the address specified by the first read address generator circuit 4 has discontinuous points (where the passing or cyclic delay occurs) at, for example, ta, tb. tc, ... as shown in Fig. 6a depending on the phase of the audio signal, and similarly the PCM digital data read from the address specified by the second read address generator circuit 5 which differs in

read timing by 1/2 the ring memory has discontinuous points at intermediate points between the discontinuous points shown in Fig. 6a, or at ta′ between ta and tb, tb′ between tb and tc, ... as shown in Fig. 6b. In Fig. 6, for convenience of explanation, the digital data is shown in an analog manner. The PCM digital data at these discontinuous points become impulse noise. Thus, to reduce this noise, the prior art used the cross-fade method. In this method, if the waveforms shown in Figs. 6a and 6b are expressed by F1(t) and F2(t), respectively, and the weighting coefficients of the attenuators 19 and 20 by $\alpha 1(t)$ and $\alpha 2(t)$, respectively, these waveform are usually weighted by the functions $\alpha 1(t)$, $\alpha 2(t)$ which have the relation, $\alpha 1(t) + \alpha 2(t) = 1$ as shown in Figs. 6c and 6d so that the impulse noise can be eliminated at the discontinuous points, and that $\alpha 1(t) \cdot F1(t) + \alpha 2(t) \cdot F2(t)$ can be obtained as the final output waveform (Fig. 6e). In this method, however, although the impulse noise at the discontinuous points can be eliminated, the pitch converted output waveform (the final output waveform) has an AM modulated component as shown in Fig. 6e.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to make it possible to smoothly connect the read addresses without occurrence of the AM modulated component at the discontinuous points due to the passing or cyclic delay between the addresses in the cross-fade method, by detecting the in-phase zero-cross position of audio data on the now-beginning side of the two read address generator circuits different in read timing by 1/2 the ring memory from each other, detecting the in-phase zero-cross position of audio data on the other now-finally generating read address generator circuit side, and controlling the read address from the switching-to-memory read address generator circuit at the connection point so that the read addresses from the address generator circuits can be connected at the in-phase zero-cross position, before the occurrence of the discontinuous points.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of one embodiment of a pitch shift apparatus of this invention.

Fig. 2 is a waveform diagram useful for explaining the operation of each portion of the embodiment of Fig. 1.

Fig. 3 is a block diagram of a conventional pitch shift apparatus.

Fig. 4 is a schematic diagram useful for explaining the basic principle of the operation of the pitch shift apparatus.

Fig. 5 is a schematic diagram useful for explaining the write address and read address to the memory.

Fig. 6 is a waveform diagram useful for explaining the operation of each portion of the conventional pitch shift apparatus shown in Fig. 3.

DESCRIPTION OF THE PREFERRED DMBODIMENT

One embodiment of this invention will be described with reference to the accompanying drawings.

Referring to Fig. 1, there are shown the A/D converter, for converting an analog signal to a PCM digital signal (of 16 bits in this embodiment), the memory 2 formed of RAM acting as a ring memory, the memory write address generator circuit 3, the first memory read address generator circuit 4, the second memory read address generator circuit 5, a first latch circuit 6 for latching data read by said first memory read address generator circuit 4, a second latch circuit 7 for latching data read by the second memory read address generator circuit 5, a first selector circuit 8 for selecting one of the data from the latch circuits 6 and 7, and the D/A converter 9 for converting the digital data from the first selector circuit 8 into an analog signal. There is also shown a second selector circuit 10 for selecting such read address from the first or second memory read address generator circuit 4, 5, that analog data corresponding to the digital data read from that address of the memory 2 is now being finally produced through the first selector 8 and D/A converter 9. In addition, shown at 11 is an address difference detection circuit which detects the difference between the address from the memory write address generator circuit 3 and the address from the first or second memory read address generator circuit 4, 5 selected by the selector circuit 10 and produces a pulse when the address difference is a predetermined value. Shown at 12 is a first flip flop F/F circuit for data inversion which is controlled by the output from the address difference detection circuit 11, and 13 is a third selector circuit for selecting the MSB (most significant bit), YD15 ((b) in Fig. 2) or ZD15 ((d) in Fig. 2) of the data which was read by the memory read address generator circuit 4 or 5 that is now going to be switched to, and stored in the latch circuit 6 or 7. Shown at 14 is a second F/F circuit which has a data input to which the output from the first F/F circuit 12 is supplied and a clock input to which the output from the third selector circuit 13 is supplied, and 15 is a third F/F circuit which has a data input to which the output from the second F/F circuit 14

and a clock input to which the output from the third selector circuit 13 is supplied. Shown at 16 is a first NAND circuit for producing the logical product of the inverted output $\overline{Q}$ of the second F/F circuit 14 and the output Q of the third F/F circuit 15, and 17 is a second NAND circuit for producing the logical product of the output Q of the second F/F circuit 14 and the inverted output $\overline{Q}$ of the third F/F circuit 15. The outputs from the first and second NAND circuits 16, 17 control the first and second memory read address generator circuits 4, 5 to increase the addresses to the memory 2, respectively.

Fig. 2 is a waveform diagram useful for explaining the operation of each portion of the pitch shift apparatus shown in Fig. 1. The analog waveforms shown in Fig. 2 at (a) and (c) for convenience of explanation are actually digital data.

The operation of the pitch shift apparatus of this embodiment will be described with reference to Figs. 1 and 2.

As mentioned above, if the digital data read by the first and second memory read address generator circuits 4, 5 and then read from the first and second latch circuits 6, 7 are converted into analog signals, the waveforms of the analog signals are as shown in Fig. 2 at (a), (c), respectively. At this time, the MSB data of the digital data which are tentatively shown in the analog waveforms in Fig. 2 at (a), (c) are offset binary codes, and thus pulses having H level in negative halves and L level in positive halves as indicated at (b), (d) in Fig. 2.

First, since the Q-output of the first F/F circuit 12 cleared by resetting is level L, and the selected signal from the third selector 13 is the first signal pulse, though the leading edge is indifinite, the Q-output of the second F/F circuit 14 becomes level L. The third selector 13 selects the MSB, ZD15 (Fig. 2 at (d)) of the output data ZD15 Q of the second latch circuit 7.

When the pitch shift operation is repeated to enter in the region (for example, when the difference between the read address and write address becomes 1/4 the ring memory) in which the cyclic delay is easy to occur, the address detection circuit 11 supplies a clock pulse to the first F/F circuit 12, causing its output (e) high level H. At this time, the output of the second F/F circuit 14, as shown in Fig. 2 at (f) is low level L, and the MSB (Fig. 2 at (d)) of the output of the second latch circuit 7 is passed through the third selector circuit 13. After the output of the first F/F circuit 12 (Fig. 2, at (e)) becomes high level H, the output of the second F/F circuit 14 (Fig. 2 at (f)) becomes at the first leading edge of the pulse (Fig. 2 at (d)). Then, the MSB, YD15 (Fig. 2 at (b)) of the output data YD15 Q of the first latch circuit 6 is produced. Moreover, after the output of the second F/F circuit 14 (Fig. 2 at (f)) becomes high level H, the output of the third F/F circuit 15 (Fig. 2 at (g)) becomes high level at the first leading edge of the pulse (Fig. 2 at (b)), and the first selector 8 produces the output data (Fig. 2 at (c)) of the second latch circuit 7 in place of the output of the first latch circuit (Fig. 2 at (a)). At this time, switching is made from the first read address generator circuit 4 to the second read address generator circuit 5. The Q-output of the second F/F circuit 14 (Fig. 2 at (f)) and the Q-output of the third F/F circuit 15, or the inversion of the output shown in Fig. 2 at (g) are supplied to the NAND circuit 17, which then produces a STOP 2 signal.

In other words, in the time difference (difference between the leading edges of pulses) between the output of the second F/F circuit 14 (Fig. 2 at (f)) and the output of the third F/F circuit 15 (Fig. 2 at (g)), or in the interval from time t2 when the digital audio signal to be read by the second read address generator circuit 5 which is going to make read operation makes zero crossing to time t1 when the digital audio signal which is now being read by the first read address generator circuit 4 which is making read operation makes in-phase zero crossing, the second read address generator circuit 5 is stopped from increasing the address. Then, from the time when switching is made from the first read address generator circuit 4 to the second read address generator circuit 5, the second read address generator circuit 5 again starts to increase the address. Thus, at time point t1, the digital audio signals can be connected in phase upon switching from the first address generator circuit 4 to the second address generator circuit 5.

When the second address generator circuit 5 repeats pitch shift operation to enter in the region (for example, the difference between the read address and the write address is 1/4 the ring memory) in which a cyclic delay to the write address generator circuit 3 is easy to occur, the clock pulse from the address difference circuit 11 is supplied to the first F/F circuit 12, so that the Q-output of the first F/F circuit 12 (Fig. 2 at (e)) is inverted to be low level L. At this time, the MSB of the output of the first latch circuit 6 (Fig. 2 at (b)) is supplied through the third selector circuit 13. When the Q-output of the first F/F circuit 12 is low level L, the output of the second F/F circuit 14 (Fig. 2 at (f)) becomes low level L at the first leading edge of the pulse (Fig. 2 at (b)), and the MSB of the output of the second latch circuit 7 (Fig. 2 at (d)) is produced. Moreover, when the output of the second F/F circuit 14 (Fig. 2 at (f)) becomes low level L, the Q-output of the third F/F circuit 15 (Fig. 2 at (g)) becomes low level L at the first leading edge of the pulse (Fig. 2 at (d)). The first selector circuit 8

produces output data of the first latch circuit 6 (Fig. 2 at (a)) in addition to the output of the second latch circuit 7 (Fig. 2 at (c)). Then, the Q-output of the third F/F circuit 15 (Fig. 2 at (g)) and the Q-output of the second F/F circuit 14, or the inversion of the output shown in Fig. 2 at (f) are supplied to the first NAND circuit 16 which then produces a STOP 1 signal. Thus, the first read address generator circuit 4 is stopped from increasing the address during the delay time between the output of the second F/F circuit 14 (Fig. 2 at (f)) and the output of the third F/F circuit 15 (Fig. 2 at (g)) (the difference between the trailing edges of the pulses). In other words, during the interval from time point t3 when the digital audio signal to be read by the first read address generator circuit 4 which is going to make read operation makes zero crossing to time point t4 when the digital audio signal which is now being read (by the second read address generator circuit 5) makes in-phase zero crossing, the first read address generator circuit 4 is stopped from increasing the address. Then, at the time when switching is made from the second read address generator circuit 5 to the first read address generator circuit 4, the first read address generator circuit 4 is again started to increase the address, thereby enabling the digital audio signals to be connected at time point t4 in phase upon switching from the second read address generator circuit 5 to the first read address generator circuit 4.

While, in this embodiment, connection is made, or switching is made, at the zero-cross point where the data is changed from positive to negative phase, the switching may of course be made at the zero-cross point where data is changed from negative to positive phase.

Thus, according to this invention, the two read address generator circuits are controlled at the connection in order that the read addresses can be connected at the in-phase zero-cross point of the audio data, thereby avoiding at the connection the generation of the AM modulated components which appear in the cross fade method due to the passing between the addresses or cyclic delay that is caused by the difference between the interval of time in which the audio data is written in the memory and the interval of time in which it is read therefrom. This follows that smooth connection of audio data can be made by only the addition of a simple control circuit for the read address generation circuits without any complicated cross fade circuit, and with the use of only one D/A converter, resulting in great reduction of cost.

Claims

1. Pitch shift apparatus comprising:
an A/D converter (1) for converting an analog audio signal to a PCM digital data;
a memory (2) provided after said A/D converter (1) so that said PCM digital data are written in and read from said memory (2);
a write address generator circuit (3) for setting a write address to said memory (2);
a first memory read address generator circuit (4) for permitting said PCM digital data written in said memory (2) to be read at a predetermined pitch;
a second memory read address generator circuit (5) which is provided in parallel with said first memory read address generator (4) and starts its reading operation by generating an address that differs by an equivalent for a 1/2 ring memory from the address which said first memory read address generator circuit (4) generates;
first and second latch circuits (6, 7) connected in parallel for latching data read from said memory (2) by said first and second read address generator circuits (4, 5);
a first selector (8) for selecting out of output data from said first latch circuit (6) and output data from said second latch circuit (7);
a D/A converter provided after said first selector (8) so as to convert digital data into an analog signal;
a second selector (10) for selecting the read address which one of said first and second memory read address generator circuits (4, 5) is now generating to read the final output data;
an address difference detecting circuit (11) for detecting the difference between the read address from said second selector (10) and a write address;
a first F/F circuit (2) provided in series with said address difference detecting circuit (11) and controlled by the output of said address difference detecting circuit (11) to be inverted;
a third selector circuit (13) for selecting the most significant bit of the output data from said first or second latch circuit (6, 7) which is associated with the data to be switched to;
a second F/F circuit (14) having a clock input to which the output of said third selector circuit (13) is supplied, and a data input to which the output of said first F/F circuit (12) is supplied;
a third F/F circuit (15) having a data input to which the output of said second F/F circuit (14) is supplied, and a clock input to which the output of said third selector circuit (13) is supplied, the output of said third F/F circuit (15) being supplied as a switching signal to said first and second selector circuits (8, 10);
a first NAND circuit (16) for producing the logical product of the inverted output of said second F/F circuit (14) and the output of said third F/F circuit (15) and thereby controlling said frist and address generator circuit (4) to increase the address; and

a second NAND circuit (17) for producing the logical product of the inverted output of said third F/F circuit (15) and the output of said second F/F circuit (14) and thereby controlling said second read address generator circuit (5) to increase the address.

2. Pitch shift apparatus comprising:
an A/D converter (1) for converting an analog audio signal to digital data;
a memory (2) for storing said digital data from said A/D convertor (1);
a write address generator circuit (3) for setting a write address to said memory (2);
a first memory read address generator circuit (4) for permitting said digital data written in said memory (2) to be read at a predetermined pitch;
a second memory read address generator circuit (5) which starts its reading operation by generating an address that differs from the address which said first memory read address generator circuit (4) generates;
a first latch circuit (6) for latching data read from said memory (2) by said first read address generator circuit (4);
a second latch circuit (7) for latching data read from said memory (2) by said second read address generator (5);
a first selector circuit (8) for selecting one of output data from said first latch circuit (6) and output data from said second latch circuit (7);
a D/A converter (9) for converting digital data from said first selector circuit (8) into an analog signal;
a second selector circuit (10) for selecting the read address which is generated from said first or second read address generator circuit (4, 5) and used so that the digital data selected by and produced from said first selector (8) is now being read;
an address difference detecting circuit (11) for detecting the difference between the read address from said second selector circuit (10) and a write address from said write address generator circuit (3) and producing a pulse when said difference becomes a predetermined value;
a first F/F circuit (12) of which the output is inverted by said pulse from said address difference detecting circuit (11);
a third selector circuit (13) for selecting the most significant bit of the output digital data from said first or second latch circuit (6, 7) which is associated with the data to be switched to;
a second F/F circuit (14) having a clock input to which the output of said third selector circuit (13) is supplied, and a data input to which the output of said first F/F circuit (12) is supplied;
a third F/F circuit (15) having a data input to which the output of said second F/F circuit (14) is supplied, and a clock input to which the output of said third selector circuit (13) is supplied;
a first NAND circuit (16) for producing the logical product of the inverted output of said second F/F circuit (14) and the output of said third F/F circuit (15); and
a second NAND circuit (17) for producing the logical product of the inverted output of said third F/F circuit (15) and the output of said second F/F circuit (14);
whereby when switching is made from said first read address generator circuit (4) to said second read address generator circuit (5), said second read address generator circuit (5) is stopped by the output of said second NAND circuit (17) from increasing the read address during the interval from time t2 at which the digital data read by said second read address generator circuit (5) makes zero crossing to time t1 at which the digital data read by said first read address generator circuit (4) makes in-phase zero crossing, in which case at said time t1, switching is made from said first read address generator circuit (4) to said second read address generator circuit (5), and when switching is made from said second read address generator circuit (5) to said first read address generator circuit (4), said first read address generator circuit (4) is stopped by the output of said first NAND circuit (16) from increasing the read address during the interval from a time point t3 at which the digital data read by said first read address generator circuit (4) makes zero crossing to a time point t4 at which the digital data read from said second read address generator circuit (5) makes in-phase zero crossing, in which case at said time point t4 switching is made from said second read address generator circuit (5) to said first read address generator circuit (4).

3. Pitch shift apparatus according to Claim 2, wherein said memory (2) is constructed to make a ring memory operation, and the read address which said first read address generator circuit (4) generates and the read address which said second read address generator circuit (5) generates are shifted from each other by an amount corresponding to 1/2 the ring memory.

4. Pitch shift apparatus according to Claim 2, wherein said memory (2) is constructed to make a ring memory operation, and said address difference detecting circuit (11) produces the pulse when the difference between the write address and the read address becomes an amount corresponding to 1/4 the ring memory.

5. Pitch shift apparatus comprising:
an A/D converter (1) for converting an analog audio signal to digital data;
a memory (2) for storing said digital data from said A/D convertor (1);
a write address generator circuit (3) for setting a write address to said memory (2);

a first memory read address generator circuit (4) for permitting said digital data written in said memory (2) to be read at a predetermined pitch;
a second memory read address generator circuit (5) which starts its reading operation by generating an address that differs from the address which said first memory read address generator circuit (4) generates; and
a D/A converter (9) for converting the digital data read from said memory (2) into an analog signal;
whereby when switching is made from said first read address generator circuit (4) to said second read address generator circuit (5), said second read address generator circuit (5) is stopped from increasing the read address during the interval from time t2 at which the digital data read by said second read address generator circuit (5) makes zero crossing to time t1 at which the digital data read by said first read address generator circuit (4) makes in-phase zero crossing, in which case at said time t1, switching is made from said first read address generator circuit (4) to said second read address generator circuit (5), and when switching is made from said second read address generator circuit (5) to said first read address generator circuit (4), said first read address generator circuit (4) is stopped from increasing the read address during the interval from a time point t3 at which the digital data read by said first read address generator circuit (4) makes zero crossing to a time point t4 at which the digital data read from said second read address generator circuit (5) makes in-phase zero crossing, in which case at said time point t4 switching is made from said second read address generator circuit (5) to said first read address generator circuit (4).

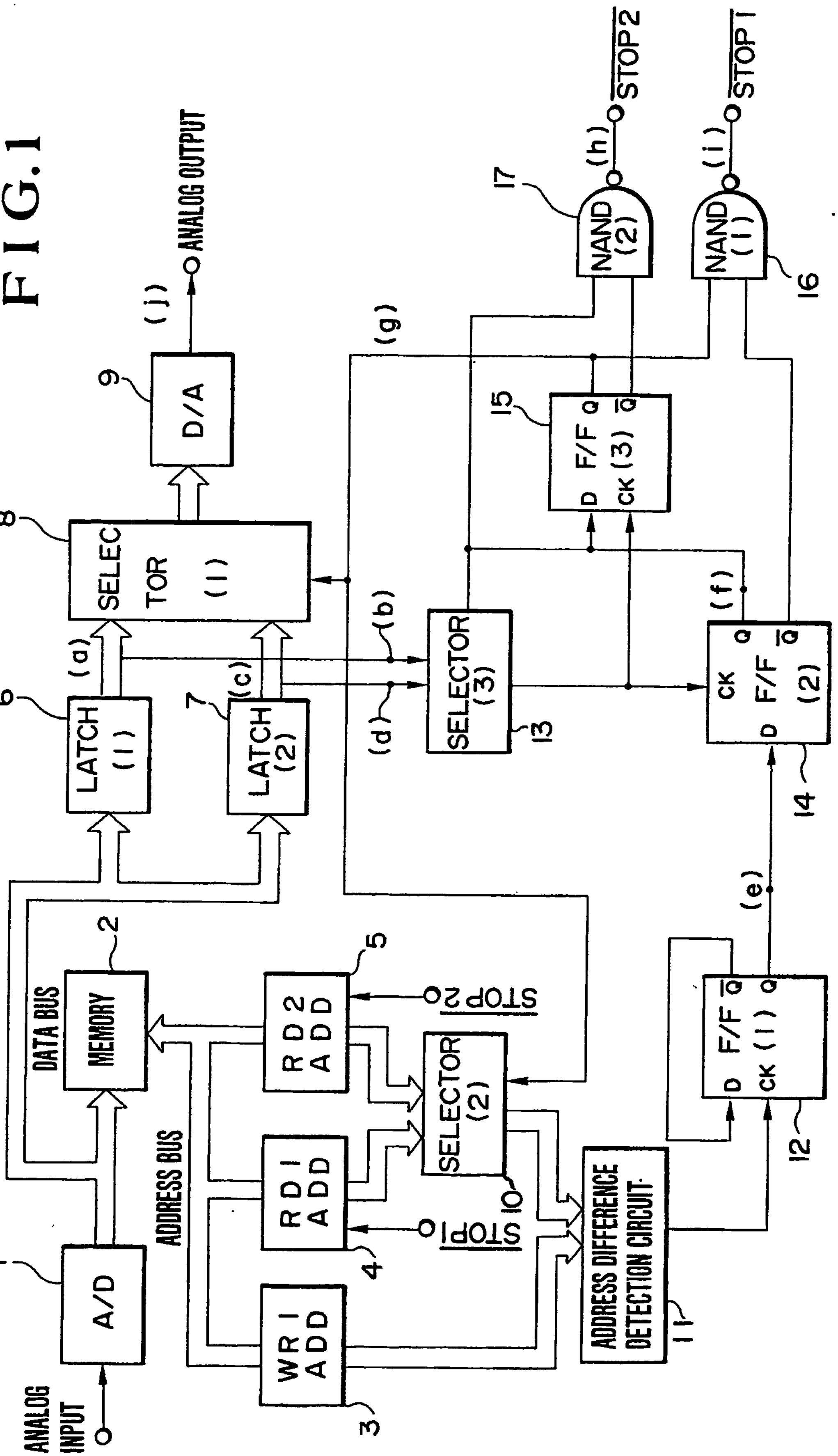

ANALOG INPUT
A/D
MEMORY
DATA BUS
ADDRESS BUS
WR 1 ADD
RD 1 ADD
RD 2 ADD
STOP1
STOP2
SELECTOR (2)
ADDRESS DIFFERENCE DETECTION CIRCUIT
F/F (1)
LATCH (1)
LATCH (2)
SELECTOR (1)
SELECTOR (3)
F/F (2)
F/F (3)
D/A
ANALOG OUTPUT
NAND (1)
NAND (2)
STOP1
STOP2
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
(j)

FIG.1

FIG.2

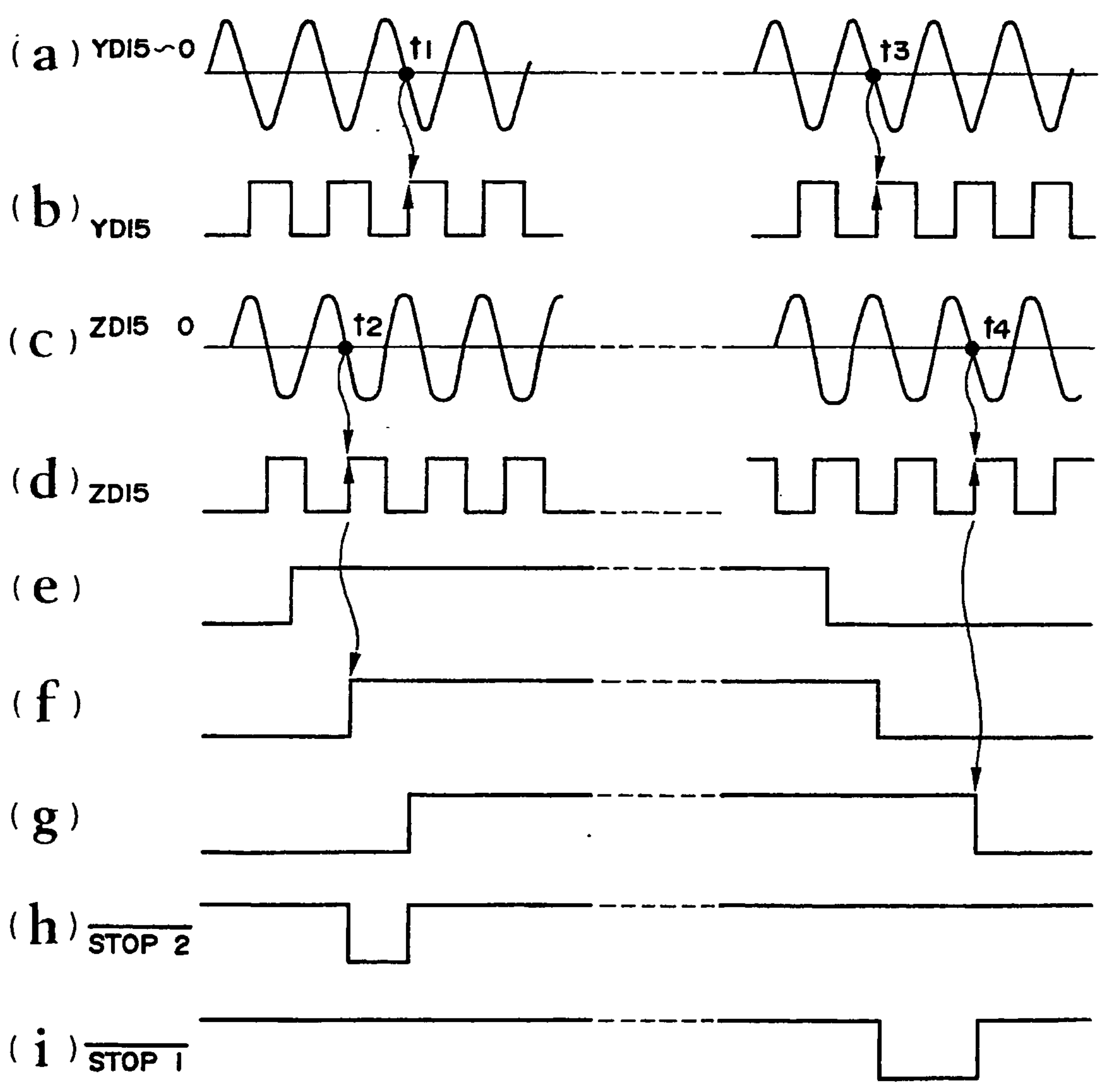


FIG.3

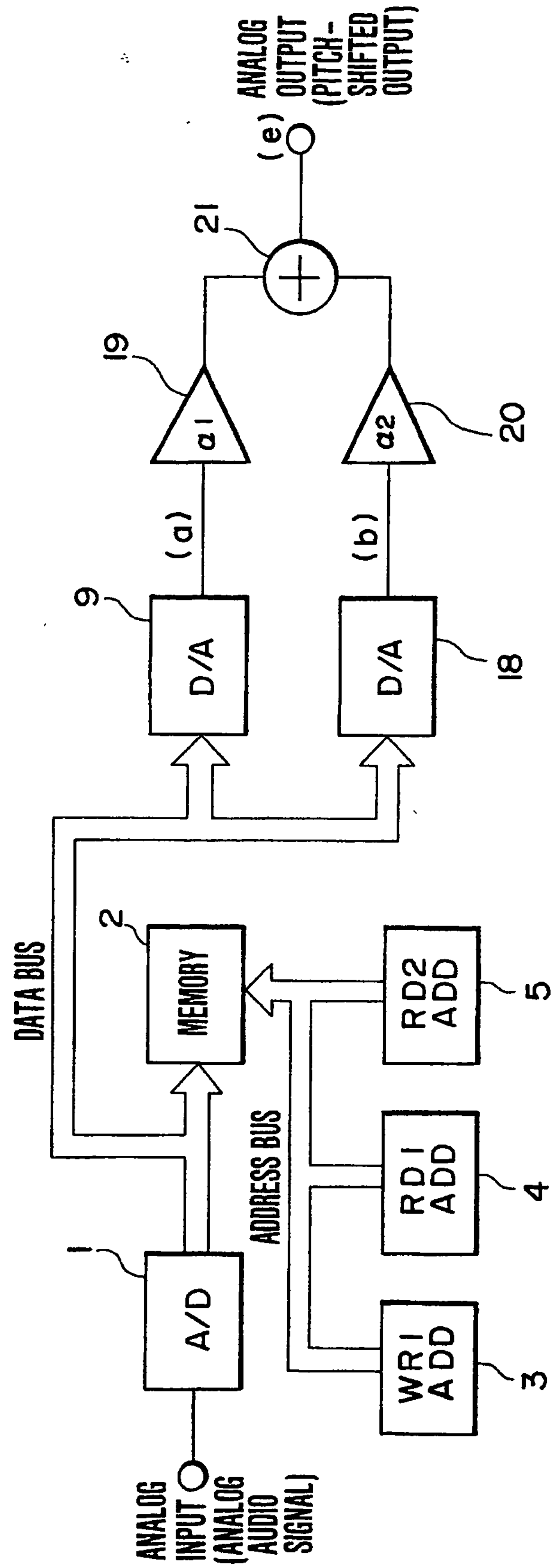

ANALOG INPUT (ANALOG AUDIO SIGNAL)
A/D
1
DATA BUS
MEMORY
2
ADDRESS BUS
WR1 ADD
3
RD1 ADD
4
RD2 ADD
5
D/A
9
D/A
18
(a)
(b)
α1
19
α2
20
21
(e)
ANALOG OUTPUT (PITCH-SHIFTED OUTPUT)

FIG.4

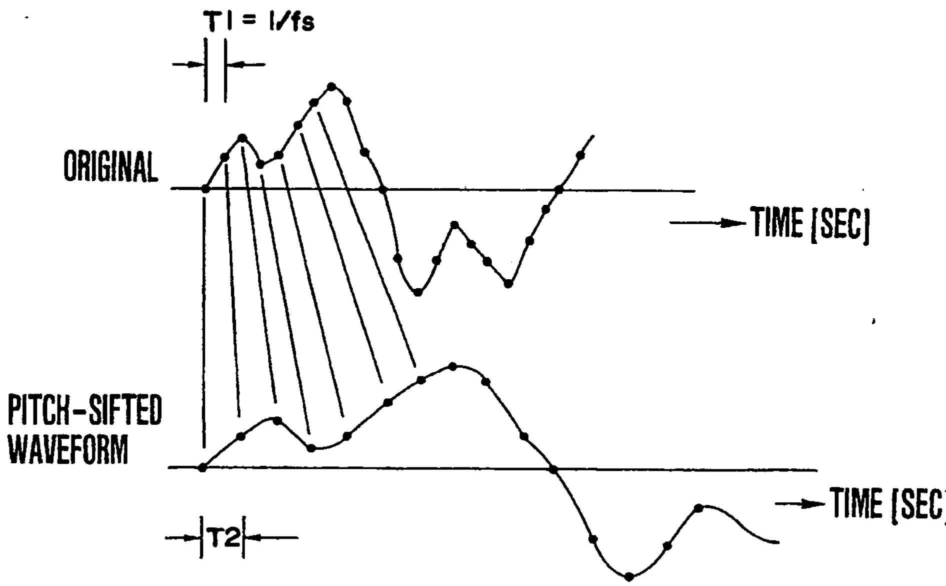
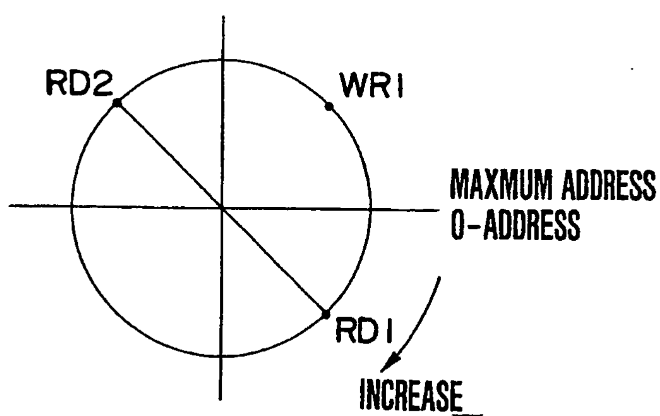

T1 = 1/fs
ORIGINAL
TIME [SEC]
PITCH-SIFTED
WAVEFORM
TIME [SEC]
T2

FIG.5


RD2
WR1
MAXMUM ADDRESS
0-ADDRESS
RD1
INCREASE

F I G.6

PRIOR ART